

### **REMARKS**

Claims 1-20 are pending. Applicant thanks the Examiner for the telephone interview held on August 18, 2004 and for agreeing that Vatinel does not teach or suggest all of the features of claim 1. By this amendment, claims 5 and 15 are cancelled and claims 1 and 11 are amended. No new matter is introduced. Support for the amendments may be found at least in Figures 1-2 and on page 4, lines 12-16, page 5, lines 14-18, page 9, line 20, and page 10, line 9 of the specification. Reconsideration and allowance of all pending claims is respectfully requested in view of the preceding amendments and following remarks.

#### **Claim Objections**

Claims 5 and 15 are objected to because of informalities. Claims 5 and 15 are cancelled, rendering the objections of claims 5 and 15 moot.

#### **Claim Rejections Under 35 U.S.C. §103**

Claims 1-6, 8-16, and 18-20 are rejected under 35 U.S.C. §103 (b) over U.S. Patent 6,317,763 to Vatinel (hereafter Vatinel) in view of U.S. Patent 6,324,239 to Potter et al. (hereafter Potter). This rejection is respectfully traversed.

Claims 5 and 15 are cancelled, rendering the rejection of claims 5 and 15 moot.

Vatinel is directed to circuits, barrel shifters, and methods for manipulating a bit pattern. However, as agreed upon during the interview, Vatinel does not disclose or suggest “each logic gate receiving data inputs and control signals, wherein each data input line is connected only to a single data transistor,” as recited in amended claim 1.

The logic circuit for use in a multiplexer as recited in claim 1 uses data sharing among transistors in order to reduce the number of transistors required by each dual rail Domino logic gate. Referring to page 4, lines 12-16 of the specification, “instead of using a separate transistor for each input data line to each logic gate, only a single transistor is required in this example for a particular data input. The other data inputs are received from adjacent or other logic gates using shared data lines.” As discussed during the interview, Vatinel does not disclose or suggest the features of inputting data only to a single data transistor and enabling all of the logic gates to share the single data transistor for each data input.

Potter is directed to a multi-function shifter that uses N-nary logic and includes an operation selection and various 1-of-N multiplexers to support a variety of shift modes. However, Potter does not cure Vatinel’s defect and does not disclose or suggest “each logic gate receiving data inputs and control signals, wherein each data input line is connected only to a single data transistor,” as recited in amended claim 1. Since none of the cited references disclose or suggest each and every element of the claim, a combination of the cited references

also does not teach or suggest each and every element of the claim. Therefore, amended claim 1 is allowable.

Claims 2-4, 6, and 8-10 are allowable because they depend from allowable claim 1 and for the additional features they recite.

Regarding claim 11, for at least the same reason as noted above with respect to claim 1, Vatinel and Potter, individually and in combination, do not disclose or suggest "providing a plurality of dual rail Domino logic gates each receiving data inputs and control signals, wherein each data input line is connected only to a single data transistor," as recited in amended claim 11. Therefore, amended claim 11 is allowable.

Claims 12-14, 16, and 18-20 are allowable because they depend from allowable claim 11 and for the additional features they recite. Withdrawal of the rejection of claims 1-4, 6, 8-14, 16, and 18-20 under 35 U.S.C. §103 (a) is respectfully requested.

Claims 7 and 17 are rejected under 35 U.S.C. §103 (a) over Vatinel in view of Potter and further in view of U.S. Patent 5,961,575 to Hervin et al. (hereafter Hervin). This rejection is respectfully traversed.

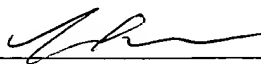
Claims 7 and 17 are allowable because they depend from allowable claims 1 and 11, respectively, and for the additional features they recite. Withdrawal of the rejection of claims 7 and 17 under 35 U.S.C. §103 (a) is respectfully requested.

In view of the above remarks, Applicant respectfully submits that the application is in condition for allowance. Prompt examination and allowance are respectfully requested.

Should the Examiner believe that anything further is desired in order to place the application in even better condition for allowance, the Examiner is invited to contact Applicant's undersigned representative at the telephone number listed below.

Respectfully submitted,

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